The demand for higher data rates is rising exponentially, requiring wider bandwidths that are only available at higher frequencies. However, circuit performance, radio channel attenuation, and power dissipation degrade at higher frequencies. These challenges are mitigated using beamforming with phased arrays and the use of high-performance semiconductors. This raises some key questions: How large antenna arrays are needed, how high data rates, and how high frequencies the current CMOS technologies supports?

This presentation focuses on the radio frequency (RF) front-end, which fundamentally determines the transmitter output power and receiver noise level. Together with bandwidth, these factors ultimately constrain the maximum data rate and link range.

Three time-domain duplexing CMOS SOI RF front-end designs are presented. The first front-end, designed for 28 GHz, utilizes the existing input matching network of a low-noise amplifier (LNA) to implement an antenna switch with minimal complexity and additional circuit area. The second front-end, also operating at 28 GHz, is part of a phased array chip that was developed to test a novel array scaling architecture. The third front-end targets 150 GHz, a frequency selected based on system-level phased array analysis to meet the 6G vision of achieving data rates exceeding 100 Gbps. This analysis is also presented, highlighting key limitations of high data rate links, primarily high power dissipation and the need for very large transmit arrays. The presentation is concluded with a 300 GHz antenna switch designed in Hiroshima university.